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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,598	07/24/2006	Hee-Seob Kim	6192.0653.US	1402

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EXAMINER	
CALEY, MICHAEL H	
ART UNIT	PAPER NUMBER
2871	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/550,598	KIM ET AL.	
	Examiner	Art Unit	
	MICHAEL H. CALEY	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-13* is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/23/05; 1/23/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto et al. (U.S. Patent No. 6,724,359 "Yamamoto").

Regarding claim 1, Yamamoto discloses a thin film transistor array panel comprising:

an insulating substrate (abstract);

a plurality of first signal lines (Figure 2 element Sn) formed on the insulating substrate;

a plurality of second signal lines (Figure 2 element G2n) insulated from the first signal lines and intersecting the first signal lines;

a plurality of first pixel electrodes (Figure 2 element 26) disposed on pixel areas defined by intersections of the first signal lines and the second signal lines and arranged in a matrix;

a plurality of first thin film transistors (Figure 2 element 40), each having three terminals connected to one of the first signal lines, one of the second signal lines, and one of the first pixel electrodes (Column 6 lines 29-65);

a plurality of second pixel electrodes (Figure 2 element 22) disposed on the pixel areas and capacitively coupled to the first pixel electrodes; and

a plurality of second thin film transistors (Figure 2 element 30), each having a terminal connected to one of the second pixel electrodes and another terminal connected to one of the first signal lines that is connected to one of the first pixel electrodes in a pixel area in an adjacent row.

Regarding claim 2, Yamamoto discloses a plurality of coupling electrodes (Figure 2, portion connecting 40 and 26) that are connected to the first pixel electrodes and overlap the second pixel electrodes while being insulated therefrom.

Regarding claim 3, Yamamoto discloses the coupling electrodes as connected to drain electrodes of the first thin film transistors connected to the first pixel electrodes (Figure 2 element 40; Column 6 lines 29-65).

Regarding claim 4, Yamamoto discloses a plurality of third signal lines (Figure 2 element G1n) intersecting the second signal lines, wherein a final terminal of each of the second thin film transistors is connected to one of the third signal lines and the second signal lines.

Regarding claim 5, Yamamoto discloses the final terminal of each of the second thin film transistors as connected to one of the third signal lines, and the thin film transistor array panel as further comprising a plurality of third thin film transistors, each having three terminals connected

to one of the second signal lines, one of the second pixel electrodes, and one of the first signal lines connected to a pixel area in an adjacent row (Figure 2 element 50).

Regarding claim 7, Yamamoto discloses a gate insulating layer (Column 6 line 53) disposed between the first signal lines and the second signal lines; and a passivation layer (Column 7 line 7) disposed between the second signal lines and the first and the second pixel electrodes, wherein the coupling electrodes are connected to the first pixel electrodes through contact holes at the passivation layer (Column 7 lines 11-14).

Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (U.S. Patent No. 6,760,082).

Lee discloses a thin film transistor array panel comprising:

an insulating substrate (Figure 4C element 202);

a plurality of first signal lines (Figure 4B element 210) formed on the insulating substrate;

a plurality of second signal lines (220) insulated from the first signal lines and intersecting the first signal lines;

a plurality of first pixel electrodes (240, left side) disposed on pixel areas defined by intersections of the first signal lines and the second signal lines and arranged in a matrix;

a plurality of first thin film transistors (230, left side), each having three terminals connected to one of the first signal lines, one of the second signal lines, and one of the first pixel electrodes;

a plurality of second pixel electrodes (240, right side) disposed on the pixel areas and capacitively coupled to the first pixel electrodes; and

a plurality of second thin film transistors (230, right side), each having a terminal connected to one of the second pixel electrodes and another terminal connected to one of the first signal lines that is connected to one of the first pixel electrodes in a pixel area in an adjacent row.

Regarding claim 2, Lee discloses a plurality of coupling electrodes (270) that are connected to the first pixel electrodes and overlap the second pixel electrodes while being insulated therefrom.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Kim et al. (U.S. Patent No. 6,473,142 "Kim").

Yamamoto fails to disclose at least one of the pixel electrodes as having at least one domain partitioning member. Kim, however, teaches a domain partitioning member on a pixel electrode (element 57) as a means of creating a multi-domain display characteristic (Column 2 lines 1-4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a domain partitioning member on at least one of the pixel electrodes. One would have been motivated to form such a domain partitioning member as a means of improving brightness and image stability at wide viewing angles (Column 2 lines 1-4).

Allowable Subject Matter

Claims 8-13 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art fails to disclose or suggest a liquid crystal display having a first and second insulating substrates, gate line, storage electrode, gate insulating layer, first and second amorphous silicon layers, data line, first source electrode, second source electrode, first and second drain electrodes, coupling electrode, passivation layer, first and second pixel electrodes, and common electrode each as proposed in claim 8.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL H. CALEY whose telephone number is (571)272-2286. The examiner can normally be reached on M-F 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael H. Caley/
Primary Examiner, Art Unit 2871